WHAT IS CLAIMED IS:

1. A content addressable memory (CAM) cell comprising:

a memory cell operable to store a bit value; and

a comparison circuit coupled to the memory cell and configured to detect the bit value stored in the memory cell, the comparison circuit including

the output transistors coupled to a match line and configured to provide a logic comparison between the stored bit and the input bit as well as drive for the match line based on the result of comparison , and

the dummy transistors coupled to a dummy line, wherein the match line and dummy line are used to detect an output value provided by the CAM cell.

2. The CAM cell of claim 1, wherein the dummy transistors has same dimension as the output transistors and are located in close proximity to the transistors driving the match line .

3. The CAM cell of claim 1, wherein the dummy transistor is turned OFF during sensing operation.

4. A content addressable memory (CAM) cell comprising:

a memory cell operable to store a bit value; and

a comparison circuit coupled to the memory cell and configured to detect the bit value stored in the memory cell, the comparison circuit including

the output transistor coupled to a match line and configured to provide a drive for the match line based on the detected bit value, and

the dummy transistors coupled to a dummy line and configured to provide a drive for the dummy line based on an inverted detected bit value, wherein the match line and dummy line are used to detect output values provided by other CAM cells also coupled to the match and dummy lines.

5. The DUMMY CAM cells, wherein the dummy transistor connected to the dummy line is approximately half the dimension(half the driving ability) of the transistors connected to the match line and is turned ON during sensing operation.

6. A Ternary content addressable memory (CAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a few pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a few pairs of dummy transistors coupled to a dummy line, wherein the match line and dummy line are used to detect an output value provided by the CAM cell.

7. The CAM cell of claim 6, wherein the dummy transistors have similar dimension as the output transistors and are located in close proximity to the output transistors.

8. The CAM cell of claim 6, wherein the dummy transistors are turned OFF during sensing operation.

9. A dummy content addressable memory (CAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a pair of dummy transistors coupled to a dummy line and configured to provide a drive for the dummy line based on an inverted detected data bit value and the detected control bit value.

10. The DUMMY CAM cell of claim 9, wherein the comparison circuit further includes the transistors connected to the dummy line has half the driving capability as those transistors connected to the match line

11. The CAM and TCAM sensing Method use the dummy match line droved by the dummy transistors in side the differential CAM or TCAM cells and also droved by the dummy transistors of the dummy CAM or TCAM cells with roughly half driving capability of the transistors inside CAM cell or dummy cam cells driving the match line.

12. The sense circuit of claim11, wherein the one dummy transistor turned ON in dummy CAM cell is approximately half the size of the remaining dummy transistors.

13. In the CAM sensing method, one row CAM or TCAM cells are connected one Dummy CAM or TCAM cells, and all these dummy CAM or TCAM cells are located In one side of CAM or TCAM array and all these dummy CAM or TCAM cells are formed on column and droved by dummy match bit line and bit line complementary.

14. In the claim 13, the data stored in the dummy CAM or dummy TCAM cells control if the row attached to that dummy cell will be enabled or disabled to be compared

15. A content addressable memory (CAM) device comprising:

an array of CAM cells arranged in a plurality of rows and a plurality of columns.

a plurality of match lines, one match line for each row of CAM cells and operatively coupled to a plurality of output transistors for the CAM cells in the row, each output transistor providing an output value indicative of a comparison result for a respective CAM cell; and a plurality of dummy lines, one dummy line for each row of CAM cells and operatively coupled to a plurality of dummy transistors for the CAM cells in the row.

16 . The CAM device of claim15, wherein each CAM cell in the array is a binary CAM cell.

17. The CAM device of claim15, wherein each CAM cell in the array is a ternary CAM cell